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MCS 51 Compatible 8-bit Microcontroller Core

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Product Specification

Introduction

Besides the well recognized desktop revolution with Personal Computers on virtually every desktop, there is another less recognized revolution with even larger impact: The embedded revolution with microcontrollers in virtually every electronic device.

Key to this technology is the availability of small yet powerful microcontrollers, most of them featuring 8bit CPUs plus additional peripherals. One of the best supported and most widely used types is Intel's MCS 51 series of devices.

Features

- Cycle compatible to MCS 51
  - Supported by a wide range of development tools
- Very compact design
  - On-chip 128byte data RAM
  - Minimum gate count
  - Optimized for FPGA implementation
- Lowest possible design risk
  - Free behavioral model
  - Comprehensive reference application
  - Synthesizable VHDL model
- Very low cost

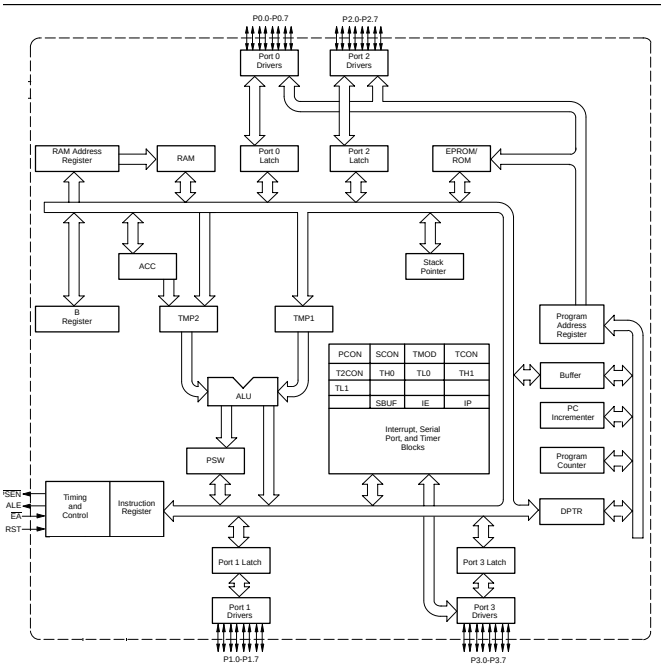

Figure 1: MCS 51 Block diagram

Compatibility

The Microcontroller Core is cycle compatible to the MCS 51 family of devices. This ensures that the Core can be used as a replacement for the original controller under all circumstances except for the following differences:

- Unlike the MCS 51 family, the Microcontroller Core does not provide any peripherals. This is due to its intended use as an FPGA solution where the features are customized to exactly fit the specification. Peripherals can be added upon requirement.
- The Microcontroller Core currently does not support interrupts, therefore RETI is not implemented.
- The MUL and DIV instruction s are performed in 2 cycles, instead of 4 used by the original MCS 51.
- The Microcontroller Core supports only a subset of the original MCS 51 SFRs. See *Table 2* for details.

	x0	x1	x2	x3	x4	x5	x6..x7	x8..xf
0x	NOP	AJMP addr	LJMP addr	RR A	INC A	INC dir	INC @Ri	INC Rn
1x	JBC bit,rel	ACALL addr	LCALL addr	RRC A	DEC A	DEC dir	DEC @Ri	DEC Rn
2x	JB bit,rel	AJMP addr	RET	RL A	ADD A,#data	ADD A,dir	ADD A,@Ri	ADD A,Rn
3x	JNB bit,rel	ACALL addr	RETI (unsupported)	RLC A	ADDC A,#data	ADDC A,dir	ADDC A,@Ri	ADDC A,Rn
4x	JC rel	AJMP rel	ORL dir,A	ORL dir,#data	ORL A,#data	ORL A,dir	ORL A,@Ri	ORL A,Rn
5x	JNC rel	ACALL addr	ANL dir,A	ANL dir,#data	ANL A,#data	ANL A,dir	ANL A,@Ri	ANL A,Rn
6x	JZ rel	AJMP addr	XRL dir,A	XRL dir,#data	XRL A,#data	XRL A,dir	XRL A,@Ri	XRL A,Rn
7x	JNZ rel	ACALL addr	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV dir,#data	MOV @Ri,#data	MOV Rn,#data
8x	SJMP rel	AJMP addr	ANL C,bit	MOVC A,@A+PC	DIV AB (2-cycle)	MOV dir,dir	MOV dir,@Ri	MOV dir,Rn
9x	MOV DPTR,#data	ACALL addr	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,dir	SUBB A,@Ri	SUBB A,Rn
Ax	ORL C,/bit	AJMP addr	MOV C,bit	INC DPTR	MUL AB (2-cycle)	reserved	MOV @Ri,dir	MOV Rn,dir
Bx	ANL C,/bit	ACALL addr	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,dir,rel	CJNE @Ri,#data,rel	CJNE Rn,#data,rel
Cx	PUSH dir	AJMP addr	CLR bit	CLR C	SWAP A	XCH A,dir	XCH A,@Ri	XCH A,Rn
Dx	POP dir	ACALL addr	SETB bit	SETB C	DA A	DJNZ dir,rel	XCHD A,@Ri	DJNZ Rn,rel
Ex	MOVX A,@DPTR	AJMP addr	MOVX A,@Ri		CLR A	MOV A,dir	MOV A,@Ri	MOV A,Rn
Fx	MOVX @DPTR,A	ACALL addr	MOVX @Ri,A		CPL A	MOV dir,A	MOV @Ri,A	MOV Rn,A

Table 1: TE-51 Instruction set

Symbol	Description
ACC	Accumulator
B	B register
DPTR	Data pointer
P0	Port 0
P2	Port 2
PSW	Program status word
SP	Stack pointer

Table 2: TE-51 SFR Map

Design Considerations

The design is fully synchronous and only requires a simple clock timing constraint for synthesis. *Table 3* lists the achieved performance data for Spartan-II devices.

Device	Maximum Frequency
XC2S200-5PQ208C	25MHz
XC2S200-6PQ208C	N/A

Table 3: TE-51 Performance

The design implements especially well on FPGA devices. *Table 4* lists the resource usage on Xilinx Spartan-II devices. Synthesis has been performed using Xilinx XST 4.1, the actual figures may vary slightly, depending on the toolchain.

Resource	Usage
Number of Slices	1,037
Number of Slice Flip Flops	353
Total Number 4 input LUTs	1,934
Number used as LUTs	1,846
Number used as route-thru	24
Number used as 32x1 RAMs	64
Number of bonded IOBs	39
Number of GCLKs	1
Number of GCLKIOBs	1
Total equivalent gate count	23,299

Table 4: TE-51 Resource Usage

References

- *Spartan-II Development System Application Note: System-on-Chip with USB*
  Trenz Electronic
  www.trenz-electronic.de
- *MCS 51 Microcontroller Family User's Manual*
  Intel Corporation

Revisions History.

Version	Date	Who	Description
0.8	00oct30	FB	First Beta
0.9	01nov04	FB	instruction set

Table 5: Revisions History.